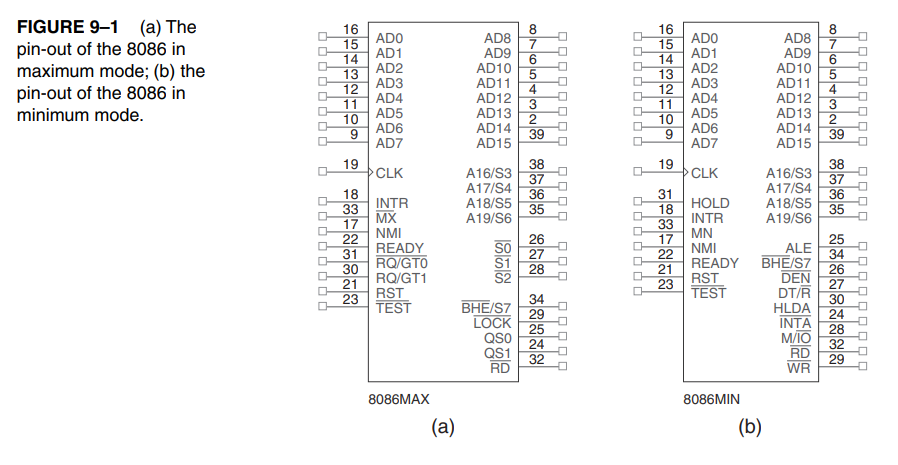
Pin Connections:



AD7–AD0:

The 8088 address/data bus lines are the multiplexed address data bus of the 8088 and contain the rightmost 8 bits of the memory address or I/O port number whenever ALE is active (logic 1) or data whenever ALE is inactive (logic 0). These pins are at their high-impedance state during a hold acknowledge.



A15–A8 :

The 8088 address bus provides the upper-half memory address bits that are present throughout a bus cycle. These address connections go to their high-impedance state during a hold acknowledge.

AD15–AD8 :

The 8086 address/data bus lines compose the upper multiplexed address/data bus on the 8086. These lines contain address bits A15–A8 whenever ALE is a logic 1, and data bus connections D15–D8 when ALE is a logic 0. These pins enter a high-impedance state when a hold acknowledge occurs.

A19/S6–A16/S3:

The address/status bus bits are multiplexed to provide address signals A19–A16 and also status bits S6–S3. These pins also attain a high-impedance state during the hold acknowledge. Status bit S6 is always a logic 0, bit S5 indicates the condition of the IF flag bit, and S4 and S3 show which segment is accessed during the current bus cycle. See Table 9–4 for the truth table of S4 and S3. These two status bits could be used to address four separate 1M byte memory banks by decoding them as A21 and A20.

RD:

Whenever the read signal is a logic 0, the data bus is receptive to data from the memory or I/O devices connected to the system. This pin floats to its high-impedance state during a hold acknowledge.

READY :

The READY input is controlled to insert wait states into the timing of the microprocessor. If the READY pin is placed at a logic 0 level, the microprocessor enters into wait states and remains idle. If the READY pin is placed at a logic 1 level, it has no effect on the operation of the microprocessor.

INTR :

interrupt request is used to request a hardware interrupt. If INTR is held high when IF = 1, the 8086/8088 enters an interrupt acknowledge cycle ( becomes active) after the current instruction has completed execution.

NMI :

The non-maskable interrupt input is similar to INTR except that the NMI interrupt does not check to see whether the IF flag bit is a logic 1. If NMI is activated, this interrupt input uses interrupt vector 2.

RESET :

The reset input causes the microprocessor to reset itself if this pin is held high for a minimum of four clocking periods. Whenever the 8086 or 8088 is reset, it begins executing instructions at memory location FFFFOH and disables future interrupts by clearing the IF flag bit.

HOLD:

The hold input requests a direct memory access (DMA). If the HOLD signal is a logic 1, the microprocessor stops executing software and places its address, data, and control bus at the high-impedance state. If the HOLD pin is a logic 0, the microprocessor executes software normally.

ALE:

Address latch enable shows that the 8086/8088 address/data bus contains address information. This address can be a memory address or an I/O port number. Note that the ALE signal does not float during a hold acknowledge.

